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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/053,707	01/24/2002	Teruhiko Kamigata	1614.1210	7916
21171	7590	03/01/2005	EXAMINER	
STAAS & HALSEY LLP SUITE 700 1201 NEW YORK AVENUE, N.W. WASHINGTON, DC 20005			INGBERG, TODD D	
			ART UNIT	PAPER NUMBER
			2124	

DATE MAILED: 03/01/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

ML

<b>Office Action Summary</b>	<b>Application No.</b> 10/053,707	<b>Applicant(s)</b> KAMIGATA ET AL.	
	<b>Examiner</b> Todd Ingberg	<b>Art Unit</b> 2124	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☒ Responsive to communication(s) filed on 24 January 2002.
- 2a) ☐ This action is **FINAL**.                      2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☒ Claim(s) 1-12 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-12 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 24 January 2002 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All    b) ☐ Some \*    c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- \* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

- |  |   |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)  | 4) <input type="checkbox"/> Interview Summary (PTO-413)<br>Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)                                   | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152)             |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)<br>Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____  |

### **DETAILED ACTION**

Claims 1 – 12 have been examined.

#### ***Priority***

1. Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

#### ***Drawings***

2. Figures 1 - 9 should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g). Corrected drawings in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

#### ***Specification***

3. The disclosure is objected to because of the following informalities: On page 87 of the Specification Figure 5 is mislabeled Figure 15. Appropriate correction is required.

#### ***Claim Rejections - 35 USC § 101***

4. 35 U.S.C. 101 reads as follows:

Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

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Claims 1 – 12 are rejected under 35 U.S.C. 101 because the claimed invention is directed to non-statutory subject matter. The claimed invention is concrete and useful but not tangible. The Examiner has provided one way to overcome this rejection.

Claim 1

A method for instruction processing **executing on a computer and stored on a computer readable medium**, comprising: a first step of identifying a classification of a functional unit which can execute a basic instruction; a second step of determining whether said basic instruction can be assigned to a logical instruction slot through checking a relationship between said classification of said functional unit and said logical instruction slot; and a third step of assigning, to an instruction slot, said basic instruction determined to be assignable to said logical instruction slot.

Claim 9

A computer program **executing on a computer and stored on a computer readable medium**, comprising: a first step of identifying a classification of a functional unit which can execute a basic instruction; a second step of determining whether said basic instruction can be assigned to a logical instruction slot through checking a relationship between said classification of said functional unit and said logical instruction slot; and a third step of assigning, to an instruction slot, said basic instruction determined to be assignable to said logical instruction slot.

***Claim Rejections - 35 USC § 103***

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

6. Claims 1 – 15 are rejected under 35 U.S.C. 103(a) as being unpatentable over USPN # 5,640,588 **Vegesna** published June 17, 1997 in view of Admitted Prior Art as Disclosed in the Background of Invention Section of the Specification.

**Claim 1**

Vegesna teaches a method for instruction processing, comprising: a first step of identifying a classification of a functional unit which can execute a basic instruction Vegesna, Abstract, Each of the instructions is classified....); a second step of determining whether said basic instruction can be assigned to a logical instruction slot through checking a relationship between said classification of said functional unit (Vegesna, Abstract, the classifications include memory reference, operations, integer operations ...) Although, Vegesna teaches classifying instructions and loading instructions. Vegesna does not explicitly teach a and said logical instruction slot ; and a third step of assigning, to an instruction slot, said basic instruction determined to be assignable to said logical instruction slot. It is APA who teaches logical instruction slot (APA, Figure 5) ; and a third step of assigning, to an instruction slot, said basic instruction determined to be assignable to said logical instruction slot (APA, figure 5). Therefore, it would have been obvious to combine the teachings of Vegesna and APA, because optimization of VLIW instructions make programs run faster.

**Claim 2**

The method for instruction processing as claimed in claim 1, wherein said first step is divided into a first sub-step of identifying an instruction category of a basic instruction (Vegesna, Abstract, classification), and a second sub-step of identifying a classification of a functional unit which can execute said instruction category (Vegesna, Abstract, classification) .

**Claim 3**

The method for instruction processing as claimed in claim 1, further comprising a step, prior to said third step, for checking a relationship between said basic instruction that can be assigned to said logical instruction slot (Figure 6) and other basic instructions to be assigned to other logical instruction slots (APA, Figure 5) .

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**Claim 4**

The method for instruction processing as claimed in claim 2, further comprising a step, prior to said third step, for checking a relationship between said basic instruction that can be assigned to said logical instruction slot and other basic instructions to be assigned to other logical instruction slots. As per claim 3.

**Claim 5**

The method for instruction processing as claimed in claim 3, wherein said second step includes a step of identifying said logical instruction slot having a lowest numeral determined to be assignable. (Interpreted to be FIFO – inherent for deterministic results).

**Claim 6**

The method for instruction processing as claimed in claim 4, wherein said third step includes a step of identifying said logical instruction slot having a lowest numeral determined to be assignable. As per claim 5.

**Claim 7**

The method for instruction processing as claimed in claim 3, wherein all of said steps are repeated for all instruction slots. (APA, Figure 6)

**Claim 8**

The method for instruction processing as claimed in claim 4, wherein all of said steps are repeated for all instruction slots. As per claim 7.

**Claim 9**

A computer program, comprising: a first step of identifying a classification of a functional unit which can execute a basic instruction; a second step of determining whether said basic instruction can be assigned to a logical instruction slot through checking a relationship between said classification of said functional unit and said logical instruction slot; and a third step of assigning, to an instruction slot, said basic instruction determined to be assignable to said logical instruction slot. As per the rejection for claim 1.

**Claim 10**

The computer program as claimed in claim 9, wherein said first step is divided into a first sub-step of identifying an instruction category of a basic instruction, and a second substep of identifying a classification of a functional unit which can execute said instruction category. As per the rejection for claim 2.

**Claim 11**

The computer program as claimed in claim 9, further comprising a step, prior to said third step, for checking a relationship between said basic instruction that can be assigned to said logical instruction slot and other basic instructions to be assigned to other logical instruction slots. As per the rejection for claim 3.

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**Claim 12**

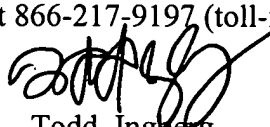
The computer program as claimed in claim 10, further comprising a step, prior to said fourth step, for checking a relationship between said basic instruction that can be assigned to said logical instruction slot and other basic instructions to be assigned to other logical instruction slots. As per the rejection for claim 4.

***Correspondence***

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Todd Ingberg whose telephone number is (571) 272-3723. The examiner can normally be reached on during the work week..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kakali Chaki can be reached on (571) 272-3719. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

  
Todd Ingberg  
Primary Examiner  
Art Unit 2124

TI